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A Methodology for Cell Merging Circuit Transformation on Post-Placement High Speed Design

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Abstract

This paper proposes a localize circuit transformation algorithm to further optimize the post-placement netlist in order to improve the overall timing of a design. The proposed algorithm reduces the total cell delay and net delay of timing violation paths by replacing a small group of cells (form up by two to three cells) that are placed close to each other with a functional equivalent standard cell available in the technology library. The algorithm has been implemented and applied to a number of optimized post-placement netlists which have went through conventional post-placement circuit transformation optimization processes such as gate relocation, cell re-sizing, repeater insertion and cell replication. The experimental results show that on average, this algorithm is able to further improve the timing of the optimized post-placement netlist by 27.75%, while keeping the design area increase by 0.2%.

Keywords: *Post-Placement Optimization, Cell Merging, Circuit Transformation, Netlist Optimization, Timing Closure*

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Background to the Study

Placement is the intermediate stage between logic synthesis and routing stages in VLSI design flow. It is also the first stage which starts the physical implementation of a design [1]. During this stage, each standard-cell in the gate-level netlist generated by the logic synthesis tool will be assigned an optimized location based on design constraints. (Ren and Dutt, 2008). With this placement information, netlist can be revisited and optimized with more accurate timing information. Netlist optimization at the post-placement stage is very important as it is able to further optimize the netlist before passing it to routing tool. Besides that, this will also provide a better starting point for routing stage. (Coudert 2002)

During post-placement optimization, placement tool will first analyse the circuit in order to identify all the timing critical paths of the design. Placement tool will then apply a variety of circuit transformation techniques such as gate relocation, cell re-sizing, repeater insertion and cell replication to reduce the negative slacks of these paths [3]. Each of these circuit transformation techniques are explained below.

1) Gate Relocation: In this technique, cells which are connected to a slow net and are placed too far to meet the timing requirement will be selected. These cells will then be move closer to shrink the span of the net [3]. The advantage of this method is that, it only focus on cells connected to critical and near-critical paths, the run time is greatly reduced compared to performing a new placement, and the optimization is more controllable .

2) Cell Re-sizing: The goal of cell re-sizing is to replace cells on the critical and near critical paths with higher power-level cells available in a library which are equivalent in functionality in order to improve timing. This is a very effective timing improving technique. It changes the input capacitances and driving resistances of cells on timing violation paths [4].

3) Repeater Insertion: Repeater serves multiple functions such as:

a) ***Signal restoration:*** Repeater is inserted at fixed wire length intervals determined by the technology to cut down delays which grow quadratically with wire length.

b) ***Strengthen the driving strength of a cell:*** Buffer can be used to increase the drive strength for a cell that is driving a large load.

c) ***Shield a critical path from high-load:*** There are two type of shielding which are isolation and partition. For isolation, cell with high fanout will be selected and buffer is inserted to buffer a portion of the fanouts to minimize the delay. For partition, buffer is used to drive the critical path load so that the driver on the critical path sees only the buffer's input pin capacitance in place of the high load.

4) Cell Replication: In this technique, the driving cell of a net is replaced by two identical replicas, and the fanouts are partitioned into two groups for each replica [4]. Its effect is similar to doubling the driver size, but at the same time it also separates the non-critical fanouts from the critical ones by connecting them to different replicas 4. This method is more effective than driver up-sizing method when a net has large non-critical load 4.

From the circuit transformation techniques described above, we can see that during post-placement optimization, placement tool tries to adjust the location or the size of cells connected to timing violation paths. Besides that, it also duplicates the high fanout cells or adds repeaters to the timing violation paths in order to reduce the negative slacks of these paths. (Michael 2006). However, there still exist some timing violation paths which are not able to improve by these circuit transformation techniques. After studying timing reports generated at post-placement optimization stage from a few netlists, we find that a few of these timing violation paths contain small group of cells which are placed close to each other and are optimizable in order to reduce the total cell delay and interconnect delay of the timing violation paths.

In this paper, we present a new circuit transformation algorithm for post-placement netlist and timing optimization. The proposed algorithm optimizes the post-placement netlist base on the placement-based timing analysis result. The algorithm goes through all the timing violation paths of the design path by path to look for cells which are placed close to each other and are replaceable with a functional equivalent cell available in the technology library. These groups of cells will then be replaced with their functional equivalent cells respectively. In order to preserve the placement of the design, the cell replacement process is done with ECO (Engineering Change Order) technique. The described algorithm has been implemented and applied to a number of post-placement netlists which have been optimized by the circuit transformation processes described above. Application results show an average of 27.75% of further timing improvement on the post-placement netlist while keeping the area increment of the design by 0.2%.

The rest of the paper is organized into five sections. In Section II, we discuss some placement-based timing analysis concept and standard cell properties in technology library. Our post-placement cell merging circuit transformation optimization algorithm is introduced in Section III. We present some experimental results in Section IV and concluding remarks in section V.

Conclusion

We have presented a new post placement circuit transformation optimization algorithm named as cell merging. This algorithm further optimizes the timing violation paths of post-placement netlist by identify the merge-able cell groups in the paths and replace it with a functional equivalent standard cell available in the data path technology libraries. Cell merging algorithm able to reduce the total cells delay and nets delay of a timing violation path, hence improve the timing of the timing violation path. As this algorithm only performs localize optimization, therefore only the cells belong to merge-able cell groups will be affected. The rest of the design will be preserved. Experimental results show an average of 27.75% of further timing improvement on the post-placement netlist while keeping the area increment of the design by 0.2%.

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